ISSN 2278 – 8875
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 2, August 2012

Signal Processing System Design on FPGA

C. Chandra Sekhar

Professor, Department of ECE, S V College of Engineering, Tirupati, A.P, India

ABSTRACT: Adaptive Digital filter based on Least Mean Square (LMS) algorithm is widely used in the field of Digital Signal processing to iteratively estimate the statistics of an unknown signal. Architecture of adaptive filter is based on three major computing elements namely multiplier, adder and delay unit to realize the Finite Impulse Response (FIR) filter. The coefficients of the FIR filter are adjusted automatically by LMS of the error so as to match the adapted output to the des ired input. This paper explains the design of adaptive filter by two approaches. One is model based approach and other is Field Programmable Gate Arrays (FPGAs). The model based design approach is developed around MATLAB, SIMULINK and SYSTEM GENERATOR tools, which provide a virtual FPGA platform. Modern FPGA include the resources needed to design efficient filtering structures. The LMS algorithm has been implemented on CYCLONE II EP2C35F672C8 FPGA device, using ALTERA QUARTUS II development platform. The three major demonstrable applications cited in the present work are System Identification, Noise reduction and Echo cancellation.

KEYWORDS: Signal Processing; LMS Adaptive Filter, FPGA

I. INTRODUCTION

Embedded Systems Design is an interdisciplinary subject, dealing with issues ranging from hardware, software, tool, algorithm and domain. The vast domain of electronics systems can be categorized into three major domains namely, Control, Communication and Computing. The objective is to understand Computing methodologies and technologies from system design perspectives in a structured approach i.e. identify study and practice platform specific tools to design, debug, and optimize electronic systems and concluding the study by implementing a project with prototype model for final demonstration.

Digital signal processing applications, falling into the computing domain of Embedded System Design, impose considerable constraints on area, power dissipation, speed and cost. Thus the design platform should be carefully chosen. The most common platforms for the design of such applications are Application Specific Integrated Circuit (ASIC), Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA). DSP can handle both fixed point and floating point mathematical tasks but cannot process high bandwidth applications due to its serial architecture. Whereas, ASIC faces lack of flexibility and require long design cycle. FPGA can makeup disadvantages of ASIC and DSP. FPGA, due to their parallel architecture, greater flexibility and speed, is a better choice for design of digital signal processing systems.

This paper investigates the applicability of Model based approaches, FPGA based approaches and combination of both as Hardware in the Loop (HIL) for adaptive filter design. In model based approach, MATLAB, Simulink, System Generator tools are used. Synthetic signal generation using equation based dynamic function and Simulink block-sets facilitate experimentation in Lab environment. In FPGA based approach the audio signal chain is established as the first step and then the Adaptive FIR filter processing block is inserted in to the chain. The hardware setup is shown in Figure-1, which include Terasic FPGA DE2 Kit, Signal generator, DSO, Altera Quartus IDE tool for HDL code compilation on computer and JTAG FPGA configuration.

The paper is organized as; section II describes the audio signal chain establishment. Section III describes the Model based signal processing. The FPGA based signal processing is covered in section-IV. Result, Conclusion and References are the concluding sections.

ISSN 2278 – 8875
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 2, August 2012

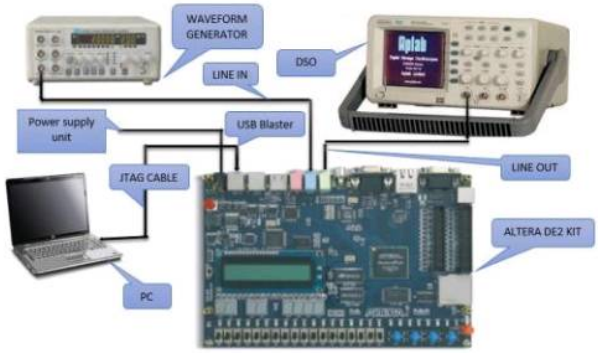

Figure 1. Signal Processing Hardware Setup using DE2 KIT

II. SIGNAL CHAIN ESTABLISHMENT

Adaptive filter design includes the selection of an adequate structure and the update algorithm. The most popular structure in adaptive signal processing is linear Finite Impulse Response (FIR) filter. Similarly, the most popular update mechanism for this structure is Least Mean Square (LMS) algorithm, developed by Bernard Widrow and Hoff [1] more than forty years ago.

Signal chain establishment [2] is the first step in the design process of digital signal processing. The analog audio signal generation, digitization using ADC section of an audio codec, Serial to parallel (SIPO), Parallel to serial (PISO), and converting back to analog signal using DAC section of audio codec are the modules of the audio signal chain as shown in Figure-2. Signal Generation can be by three methods; signal genearator equipment, digital signal synthesis in FPGA and MATLAB based signal generation. Signal generators are availble from a host of vendors in all price range. Digital signal sythesis in side FPGA logic is very useful for Hardware Description Langauge (HDL) based simulation and hardware testing. Sine waveform can be generated using simple Look Up Table (LUT) in FPGA. Numerically ontrolled Oscillator (NCO) IP cores in FPGA can be used to synthesize complex waveforms. MATLAB is an efficient modelling tool for signal generation, signal processing using analysis using virtual sink sources like oscilloscope, spectrum analyser, etc. Audio signal can be generated by playing audio files in various formats as shown in green shaded left side block in Figure 3 and Figure 4. In Adpative filter design, two signal sources are required; one for the unknown X[k] and the other for the desired D[k]. Its very handy to generate these as stereo signals using MATLAB and deliver them through headphone connector of the computer as shown in blue shaded right side block in Figure 3 and Figure 4. Artificial synthetic ECG signals shown in Fig be generated by Dynamic function. Such functions are usually equation based[3]. Echo geneartion using MATLAB simulink model [4] is shown in Figure-4.

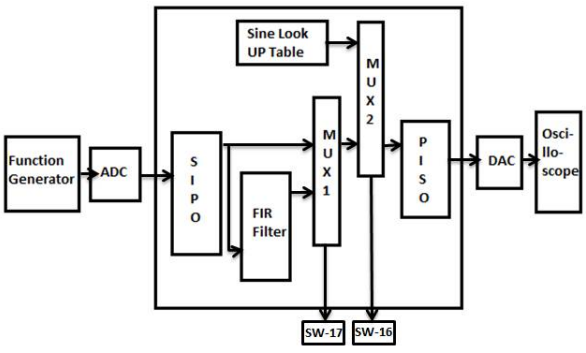

Figure 2. Establishing signal chain

ISSN 2278 – 8875
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 2, August 2012

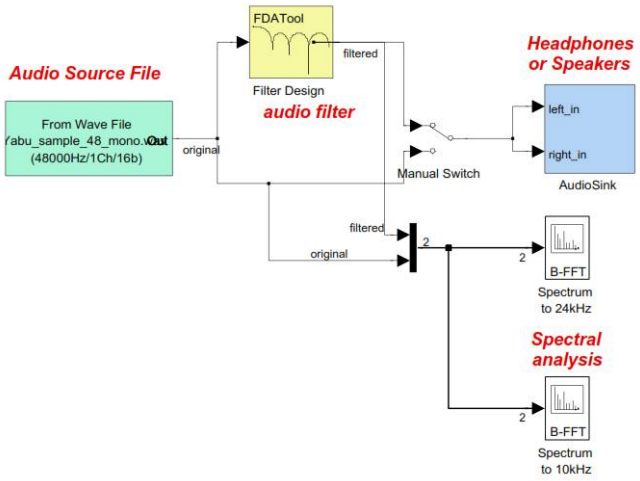

Figure 3. Simulink Models for FIR filter design

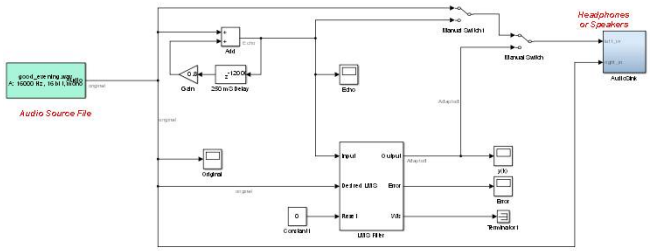

Figure 4 Simulink Models for Echo generation

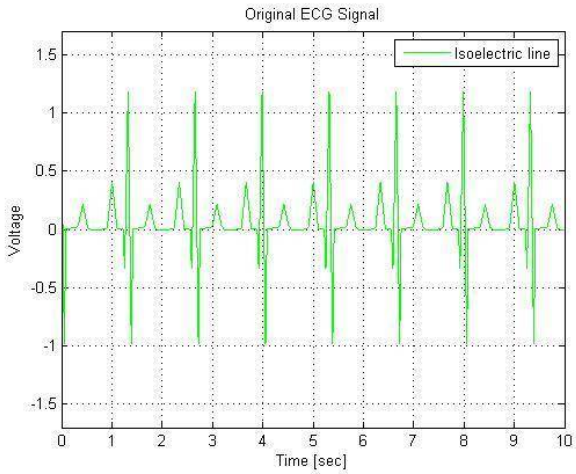

Figure 5. Dynamic function based Synthetic ECG signal

III. MODEL BASED SIGNAL PROCESSING

An ideal approach for embedded system design is model based design approach. There are many system modeling tools available from various vendors, which facilitate the design of hardware & software before actual physical implementation of the system. Model Based Design assists the design, simulation and code generation for any one of Processor/Microcontroller, DSP and FPGA platforms. MATLAB, SIMULINK tool from Mathworks and SYSTEM GENERATOR tool from Xilinx have been used in this work.

System Generator is a system level modeling tool that facilitates FPGA hardware design. It extends Simulink in many ways to provide a modeling environment that is well suited to hardware design. The tool provides high-level abstractions that are automatically compiled into an FPGA quickly. The system generator tool can be used to generate target specific, bit-true, cycle-accurate, synthesizable Verilog and VHDL code.

System Generator based single order LMS algorithm module is replicated for all the three applications; Echo cancellation, System Identification, and Noise reduction as shown in Figure 6,7,8 respectively. The step size of the

ISSN 2278 – 8875
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 2, August 2012

LMS algorithm is variable and can be adjusted to minimize the error E[k] and to get more accurate output Y[k]. The System Generator Wave Scope block used in the model provides a powerful and easy-to-use waveform viewer for analyzing and debugging. Here it allows observing the time changing analog values of the adapted coefficient of the single order LMS after the conclusion of the simulation. Figure-6 shows the system generator model of adaptive echo cancellation design [4]. Here the mux1 is used to generate the echo by adding the sine signal and the sine half signal. Mux2 is used to pass the desired signal.

Figure-7 shows the System Generator Model of System Identification design [5]. The blue shaded top block is the unknown system to be identified by the rest of the LMS algorithm blocks. Here the unknown system is kept as a single order FIR filter which basically reduces the gain of the input signal. Figure-8 shows the System Generator Model of Noise cancellation design. The signal and the noise are generated separately and then combined by an analog summer. This mixed signal is the unknown signal X[k] and the noise is the desired signal D[k]. The adapted signal Y[k] is then subtracted from the unknown signal X[k] to retrieve the noise free original signal.

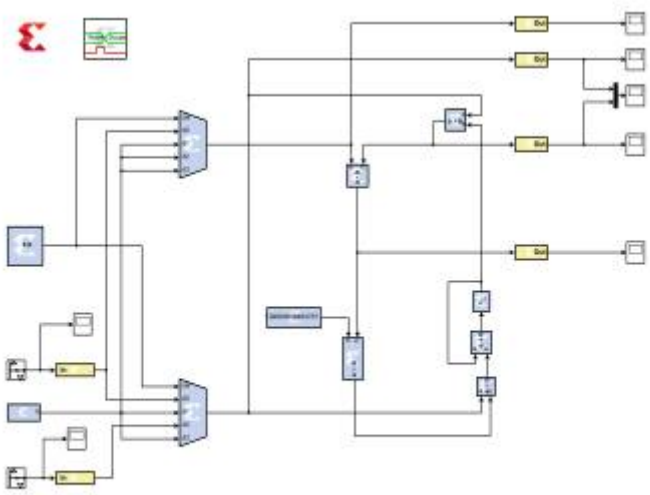

Figure 6. System Generator based Echo cancellation

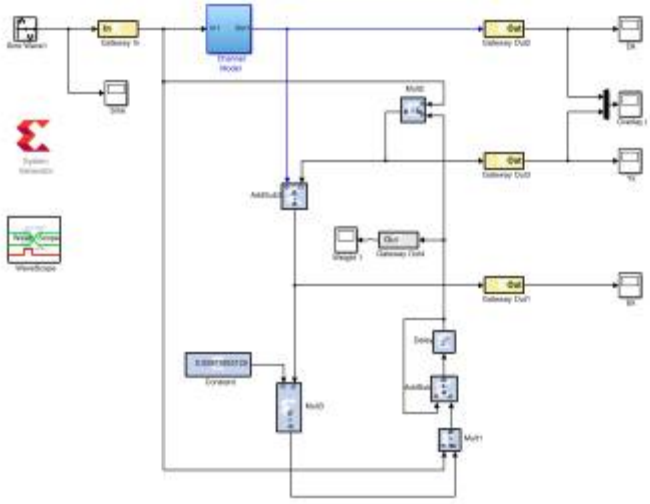

Figure 7. System Generator based System Identification

ISSN 2278 – 8875
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 2, August 2012

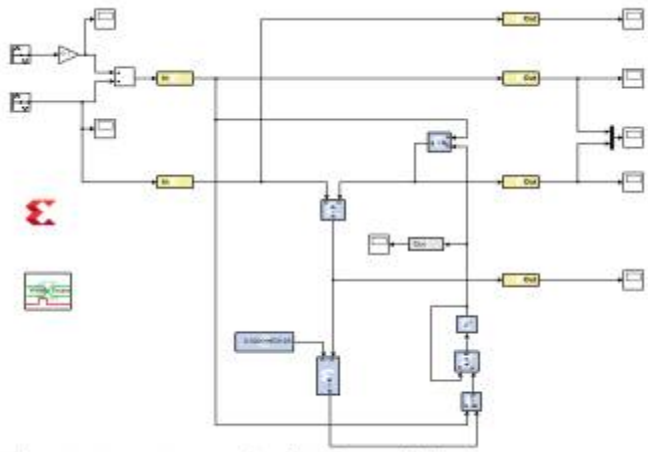

Figure 8. System Generator based Noise cancellation

IV. FPGA BASED SIGNAL PROCESSING

The data path architecture of LMS adaptive filter on FPGA is shown in Figure 9. The noise mixed signal and the noise are generated separately by the Simulink model on the host computer and taken out from the stereo audio line out of the computer. These signals are digitized by the ADC section of the stereo audio codec and available as Left/Right serial AUD_ADC_DATA signals at the audio bit clock rate and at sample clock AUD_ADC_LRCK. The serial AUD_ADC_DATA is converted to parallel by the Serial in Parallel out (SIPO) module, which is passed through the MUX 1 to select either the external or the internal noise mixed signal by the sine LUT in FPGA. The signals of the LMS Adaptive Filter X[k], D[k], Y[k] and E[k] are selected by MUX 2 for observation. MUX 3 is used for selecting the MUX 2 signal output or external unprocessed signals. The output of MUX 3 is further fed to the MUX 4 to select internal pure sine wave signal or the processed filtered signal. Since all the signal processing are done on parallel 16 bit data, so at the output port there is a Parallel In SerialOut (PISO) operation to get the output serially which is then fed to the DAC section of the on-board audio codec and finally observed on DSO.

V. RESULT

The LMS algorithm based adaptive filter was implemented on CYCLONE II EP2C35F672C8 FPGA device, using ALTERA QUARTUS II tool and Terasic DE2 Kit. The FPGA resource utilization by the three demonstrable applications cited in the present work namely System Identification, Noise reduction and Echo cancellation are given in Table –I.

VI. CONCLUSION

Present work envisages the signal generation and signal processing using both Model based approach and hardware realization on FPGA target. The complete FPGA design cycle of HDL Coding, Simulation, Synthesis, Implementation, Testing and Tabulation of FPGA resource usages by the three applications of LMS ADAPTIVE filter namely, System Identification, Noise reduction and Echo cancellation, were carried out successfully.

ISSN 2278 – 8875
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering
Vol. 1, Issue 2, August 2012

TABLE I.

Cyclone II EP2C35F672C8 Logic resources	System Identification Usage		ECG Noise Cancellation Usage		Echo Cancellation Usage	
Total Logic Elements 33216	1020	3%	1124	3%	1039	3%
Total Registers 33216	567	2%	588	2%	452	1%
Total Pins 475	312	66%	248	52%	312	66%
Total Memory bits 483840	48	1%	0	-	0	-
Total Multiplier 70	22	31%	20	29%	14	20%
Total PLL 4	1	25%	1	25%	1	25%

REFERENCES

[1] B. Widrow, J. M. McCool, M. G. Larmore and C. R. Johnson, ”Stationary and nonstationary learning characteristics of the LMS adaptive filter”, Proc. of IEEE, vol. 64, No. 8, pp. 1947-1951, August,1976.
[2] Sashank Shekhar Pujari, Prangya Paramita Muduli, Amruta Panda,Rasmita Badhai,Sofia Nayak, Yougajyoty Sahoo, Design & Implementation of FIR Filters using On-Board ADC-DAC & FPGA, International Conference on Information Communication & Embedded Systems, February 2014, Tamilnadu, India (ICICES 2014)
[3] Patrick E. McSharry_, Gari D. Clifford, Lionel Tarassenko, and Leonard A. Smith, A Dynamical Model for Generating Synthetic Electrocardiogram Signals, IEEE Transactions on Biomedical engineering, Vol. 50, No. 3, March 2003.
[4] Sashank Shekhar Pujari, Amruta Panda, P K Dash, Design & Implementation of FPGA based Adaptive Filter for Echo Cancellation, International Conference on Convergence of Technology, Pune, India (ICCT 2014)
[5] P.K. Dash, Sashank Shekhar Pujari, Er.Yougajyoty Sahoo, Design and Implementation of Single Order LMS based Adaptive System Identification on Altera Based Cyclone-II FPGA, International Conference on Communication and Signal Processing, Tamilndau, India, (ICCSP 2014).